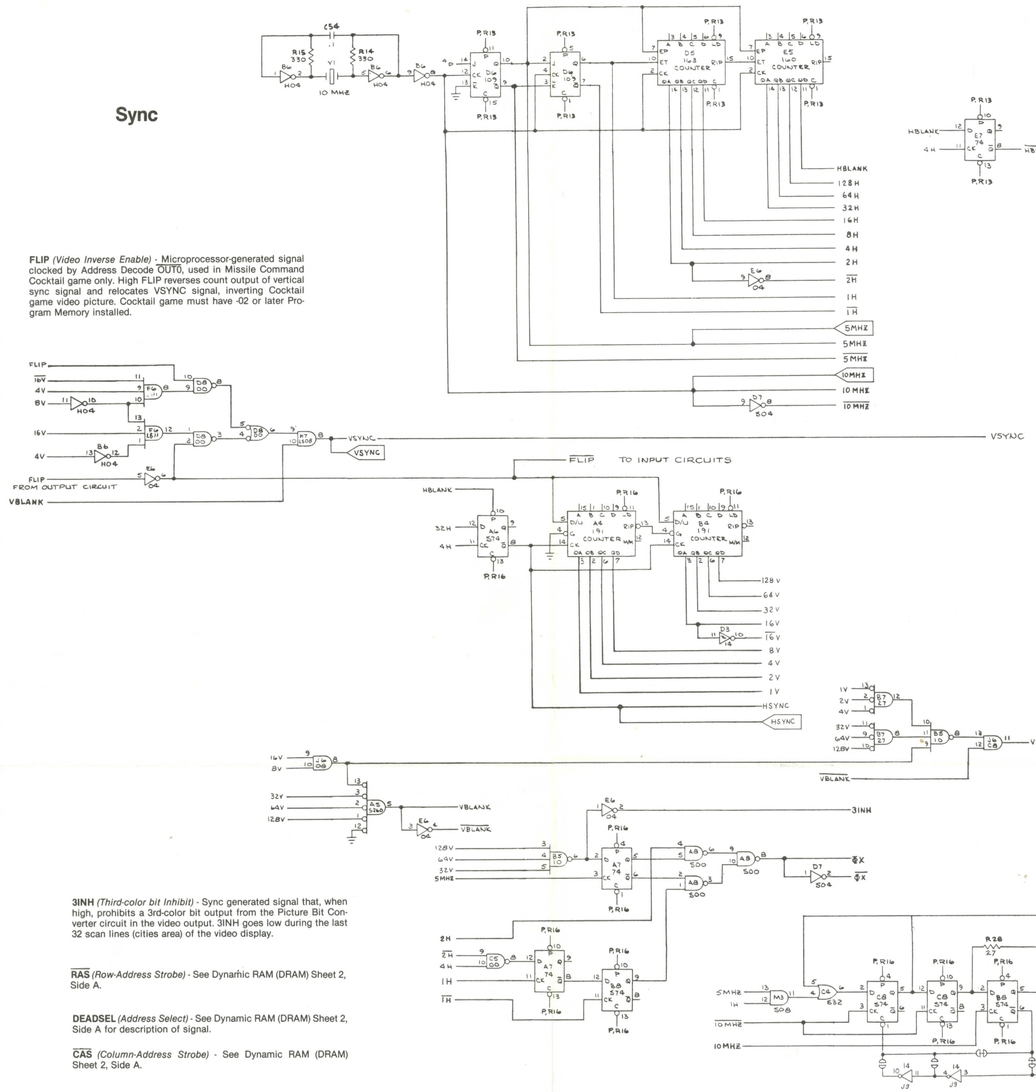
Sync



FLIP *(Video Inverse Enable)* - Microprocessor-generated signal clocked by Address Decode OUT0, used in Missile Command Cocktail game only. High FLIP reverses count output of vertical sync signal and relocates VSYNC signal, inverting Cocktail game video picture. Cocktail game must have -02 or later Program Memory installed.

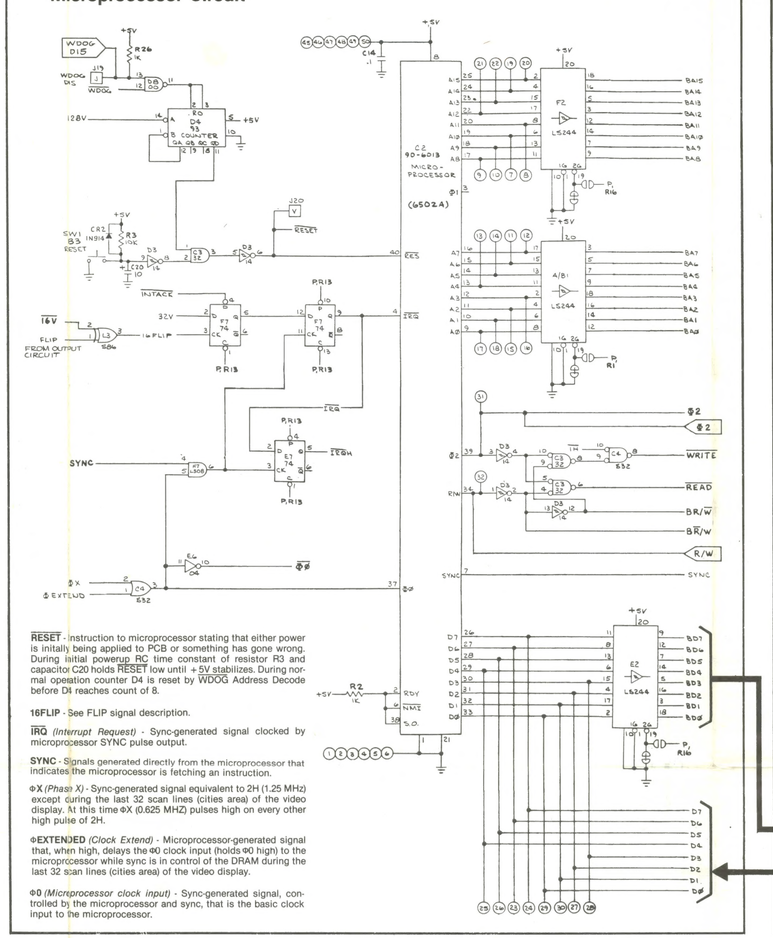
3INH *(Third-color bit Inhibit)* - Sync generated signal that, when high, prohibits a 3rd-color bit output from the Picture Bit Converter circuit in the video output. 3INH goes low during the last 32 scan lines (cities area) of the video display.

$\overline{\text{RAS}}$ *(Row-Address Strobe)* - See Dynamic RAM (DRAM) Sheet 2, Side A.

DEADSEL *(Address Select)* - See Dynamic RAM (DRAM) Sheet 2, Side A for description of signal.

$\overline{\text{CAS}}$ *(Column-Address Strobe)* - See Dynamic RAM (DRAM) Sheet 2, Side A.

Microprocessor Circuit



$\overline{\text{RESET}}$ - instruction to microprocessor stating that either power is initially being applied to PCB or something has gone wrong. During initial powerup RC time constant of resistor R3 and capacitor C20 holds $\overline{\text{RESET}}$ low until +5V stabilizes. During normal operation counter D4 is reset by $\overline{\text{WDOG}}$ Address Decode before D8 reaches count of 8.

16FLIP - See FLIP signal description.

$\overline{\text{IRQ}}$ *(Interrupt Request)* - Sync-generated signal clocked by microprocessor SYNC pulse output.

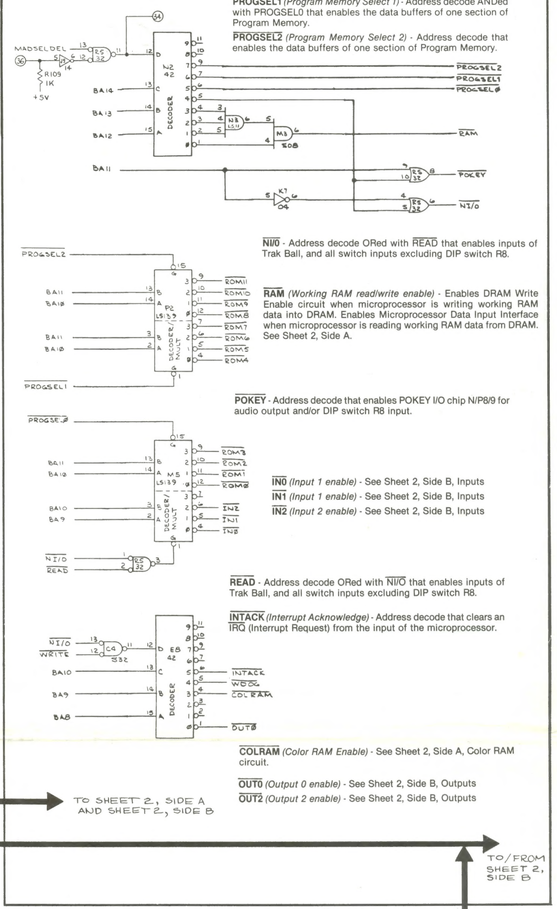
SYNC - Signals generated directly from the microprocessor that indicates the microprocessor is fetching an instruction.

ΦX *(Phase X)* - Sync-generated signal equivalent to 2H (1.25 MHz) except during the last 32 scan lines (cities area) of the video display. At this time ΦX (0.625 MHZ) pulses high on every other high pulse of 2H.

ΦEXTENDED *(Clock Extend)* - Microprocessor-generated signal that, when high, delays the Φ0 clock input (holds Φ0 high) to the microprocessor while sync is in control of the DRAM during the last 32 scan lines (cities area) of the video display.

Φ0 *(Microprocessor clock input)* - Sync-generated signal, controlled by the microprocessor and sync, that is the basic clock input to the microprocessor.

Address Decoding



$\overline{\text{PROGSEL0}}$ *(Program Memory Select 0)* - Address decode ANDed with PROGSEL1 that enables the data buffers of one section of Program Memory.

$\overline{\text{PROGSEL1}}$ *(Program Memory Select 1)* - Address decode ANDed with PROGSEL0 that enables the data buffers of one section of Program Memory.

$\overline{\text{PROGSEL2}}$ *(Program Memory Select 2)* - Address decode that enables the data buffers of one section of Program Memory.

$\overline{\text{NI0}}$ - Address decode ORed with $\overline{\text{READ}}$ that enables inputs of Trak Ball, and all switch inputs excluding DIP switch R8.

RAM *(Working RAM read/write enable)* - Enables DRAM Write Enable circuit when microprocessor is writing working RAM data into DRAM. Enables Microprocessor Data Input Interface when microprocessor is reading working RAM data from DRAM. See Sheet 2, Side A.

$\overline{\text{POKEY}}$ - Address decode that enables POKEY I/O chip N/P8/9 for audio output and/or DIP switch R8 input.

$\overline{\text{IN0}}$ *(Input 1 enable)* - See Sheet 2, Side B, Inputs
$\overline{\text{IN1}}$ *(Input 1 enable)* - See Sheet 2, Side B, Inputs
$\overline{\text{IN2}}$ *(Input 2 enable)* - See Sheet 2, Side B, Inputs

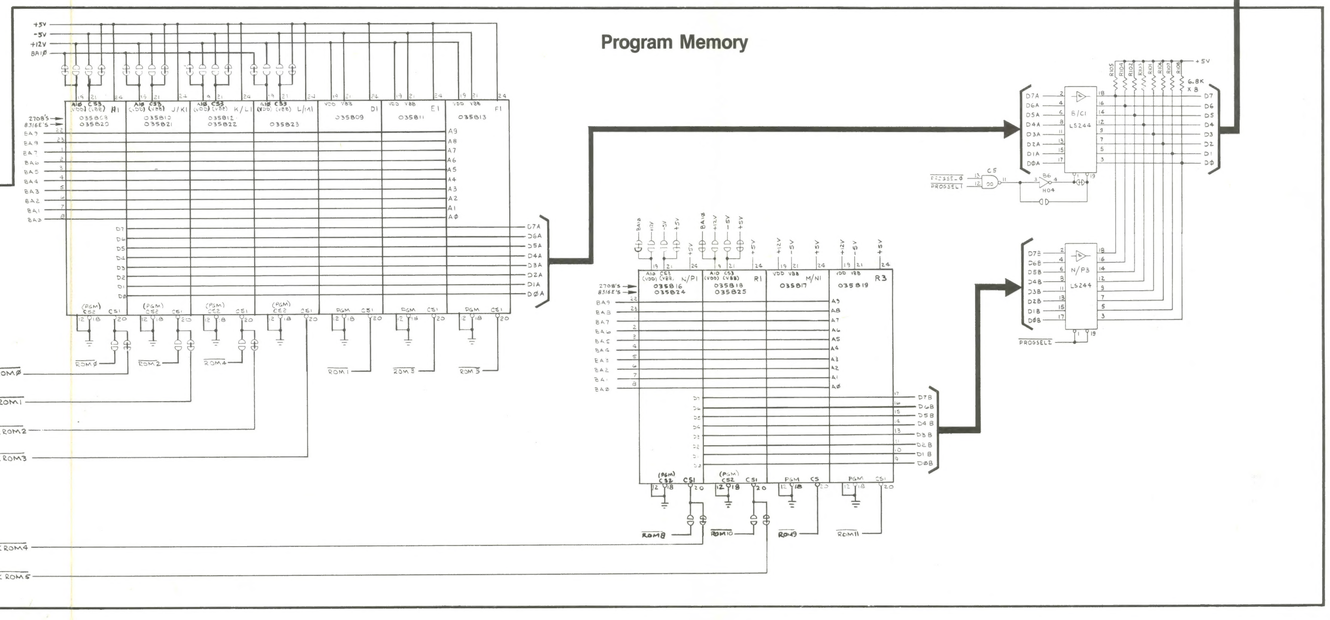
$\overline{\text{READ}}$ - Address decode ORed with $\overline{\text{NI/O}}$ that enables inputs of Trak Ball, and all switch inputs excluding DIP switch R8.

$\overline{\text{INTACK}}$ *(Interrupt Acknowledge)* - Address decode that clears an $\overline{\text{IRQ}}$ (Interrupt Request) from the input of the microprocessor.

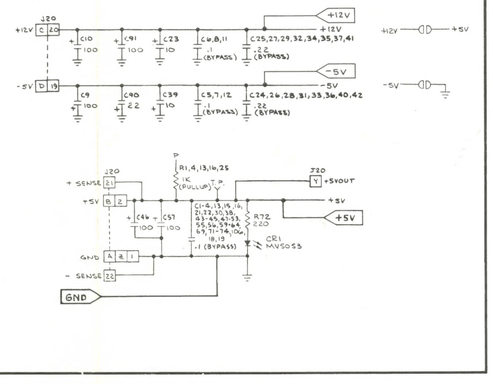
$\overline{\text{COLRAM}}$ *(Color RAM Enable)* - See Sheet 2, Side A, Color RAM circuit.

$\overline{\text{OUT0}}$ *(Output 0 enable)* - See Sheet 2, Side B, Outputs
$\overline{\text{OUT2}}$ *(Output 2 enable)* - See Sheet 2, Side B, Outputs

Program Memory



Power Input



Sheet 1, Side B

MISSILE COMMAND™

Microprocessor

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